Low-cost FPGA implementation of 2D digital pre-distorter for concurrent dual-band power amplifier

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Abstract

This paper proposes a low-cost hardware architecture based on concurrent dual-band digital pre-distorter (DPD). The architecture is implemented on field programmable gate array (FPGA) to compensate for the nonlinearity of the concurrent dual-band power amplifier (PA). This implementation introduces a novel model complexity reduction technique into system, namely, time-division multiplexing for out-of-band lookup tables (LUTs) sharing. Performances are evaluated with an experimental test setup using a wideband class-F PA. The dual-band signal center frequency separated by 80 MHz. Lower and upper center frequency are located at 2.61 GHz and 2.69 GHz, respectively. This novel DPD implementation maintains excellent performance, but uses hardware resources reduced by 29.17% compared with conventional approaches. The results show that the adjacent channel power ratio (ACPR) is less than \(-59\) dBc and normalized mean square error (NMSE) is around \(-62\) dB for lower sideband (LSB) and \(-63\) dB for upper sideband (USB).

Keywords: power amplifier, concurrent dual-band, digital predistorter, lookup table, field programmable gate array (FPGA)

1 Introduction

Wireless communication system is experiencing a rapid development. Wireless communication standard is no longer single. Wideband code division multiple access (WCDMA), orthogonal frequency division multiplexing (OFDM) and other modulation schemes have been applied to communication system now. The multi-standard coexistent situation makes it a hot research that one PA affords to transmit dual-band signal concurrently in Ref. [1]. The technology significantly reduces costs and the number of components in the base station, which is accordant with the concept of green communication. Since these modulation modes of high spectrum utilization are almost based on non-constant envelope, signal will reveal a high peak-to-average-power ratio (PAPR). PA stimulated by such signal will create harder nonlinearities. So it is desirable to obtain a reasonable tradeoff between the linearity and the power efficiency.

Digital pre-distortion technique is a low-complexity and high-accuracy method to linearize PA in Ref. [2]. This technique improves the linearity in the high-efficiency region of PA. Nevertheless, it cannot be achieved perfect effect if conventional pre-distortion technique is applied to concurrent dual-band PA. The reason is that a dual-band signal with frequency separation ranges from several hundred MHz to several GHz, while digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) run at 5 to 7 times of signal bandwidth, generally, which greatly increases the costs of concurrent dual-band transceiver.

Bassam et al. propose a concurrent dual-band digital pre-distortion model and explain mathematical manipulations from memory polynomial to two-dimensional (2D)-DPD in detail in Ref. [1]. This 2D-DPD model reaches very good distortion compensation showing ACPR of usually less than \(-50\) dBc and NMSE around \(-40\) dB. LUT, as an effective technique to implement digital predistortion model, is widely used in the hardware
design because it uses less hardware resources. Cesari et al. propose the basic pre-distortion cell (BPC) structure in Ref. [3]. This structure is mainly composed of LUTs. The DPD can be mapped into the FPGA as a set of cascaded BPC cells. 2D-LUT is explored by Ding et al. in Ref. [4]. But 2D-LUT has much higher complexity. To simplify the complexity of this architecture, Ding et al. transform it into one-dimensional. This one-dimensional architecture saves a lot of hardware resources at a cost of partial accuracy. Furthermore, on the basis of 2D-DPD, Kwan et al. propose LUT with variable depths implementation that minimizes the number of LUT entries, leading to the reduction of performance in accuracy in Ref. [5]. In Ref. [6], Quindroit et al. propose a new set of orthogonal polynomials for 2D-DPD. As an extension, in Ref. [7], they propose an efficient hardware implementation of the orthogonal polynomial 2D-DPD inside the FPGA based on time-division multiplexing technique.

This article starts with the description of the proposed concurrent dual-band 2D-DPD system model, recalls the conventional dual-band 2D-DPD architecture based on LUTs. Then, shows the proposed FPGA hardware implementation solution. Finally, illustrates the efficiency of the proposed 2D-DPD implementation solution testing on a Virtex-6 FPGA board and gives the experimental results. A conclusion is presented in the end.

2 Concurrent dual-band 2D-DPD system model and implementation solution

2.1 2D-DPD system model

The block diagram of proposed and conventional dual-band DPD system are presented in Fig. 1. This proposed architecture is different from conventional architecture shown in Ref. [5]. There are three primary DPD blocks in proposed architecture, in-band pre-distorter I and in-band pre-distorter II are used to compensate for distortion components of in-band intermodulation products, out-of-band pre-distorter is used to eliminate the nonlinear distortion of in-band cross-modulation products. The outputs of in-band pre-distorter and out-of-band pre-distorter are summed together, then converted to the analog domain by DACs and frequency up-converted by modulators. The radio frequency (RF) signals are combined using a combiner before being sent into a dual-band PA.

The dual-band PA model can be expressed as the following equations in Ref. [1]:

\[
y_1(n) = \sum_{q=0}^{Q-1} \sum_{k=0}^{K-1} \sum_{j=0}^{K_j-1} c_{1,q,k,j} x_1(n-q) x_1(n-q) \cdot x_2(n-q) \cdot x_2(n-q)
\]

(1)

\[
y_2(n) = \sum_{q=0}^{Q-1} \sum_{k=0}^{K-1} \sum_{j=0}^{K_j-1} c_{2,q,k,j} x_2(n-q) x_2(n-q) \cdot x_1(n-q) \cdot x_1(n-q)
\]

(2)

Where \(x_1(n)\) and \(x_2(n)\) are the input signals of PA at two different frequencies, respectively. \(y_1(n)\) and \(y_2(n)\) are the output signals at each band. \(c_{1,q,k,j}\) and \(c_{2,q,k,j}\) are the coefficients at each PA band. \(Q\) and \(K\) are the memory depth and nonlinearity order, respectively. The indirect learning model of dual-band DPD can be obtained from exchanging the variables \(x_1(n)\) with \(y_1(n)\) and \(x_2(n)\) with \(y_2(n)\) in Ref. [5].

In order to calculate and update the coefficients, a part of output signals of PA is fed back via attenuator which attenuates power to an appropriate value to avoid overlarge signal power. Then, two feedback signals are filtered to remove the other sideband signal. The remaining RF signals are down-converted to intermediate frequency (IF). The following filter intends to cancel mirror image generated by down-converter. The IF signals then pass.
through ADCs, and are digitalized down-conversion to baseband signals on FPGA development board. Finally, the two feedback baseband signals are time-aligned with forward original baseband signals to extract coefficients and construct LUTs by MATLAB software.

2.2 Conventional dual-band 2D-DPD architecture based on LUT

The 2D-DPD model can be written as Eq. (1) and Eq. (2). They are modified to the following equations in Ref. [5]:

\[
y_1(n) = \sum_{q=0}^{Q-1} x_1(n-q) \sum_{j=0}^{K-1} |x_1(n-q)|^j LUT_{1,m,j} \left[ |x_1(n-q)|^j \right] \tag{3}
\]

\[
y_2(n) = \sum_{q=0}^{Q-1} x_2(n-q) \sum_{j=0}^{K-1} |x_2(n-q)|^j LUT_{2,m,j} \left[ |x_2(n-q)|^j \right] \tag{4}
\]

Where

\[
LUT_{1,m,j} \left[ |x_1(n-q)|^j \right] = \sum_{k=0}^{K-1-j} c_{1,x,j,k} |x_1(n-q)|^k \tag{5}
\]

\[
LUT_{2,m,j} \left[ |x_2(n-q)|^j \right] = \sum_{k=0}^{K-1-j} c_{2,x,j,k} |x_2(n-q)|^k \tag{6}
\]

Eq. (5) and Eq. (6) completely describe the in-band pre-distorter of \( x_1(n) \) and \( x_2(n) \), respectively.

Here, in order to describe conveniently, out-of-band pre-distorter of \( x_1(n) \) and \( x_2(n) \) are expressed as follows.

\[
LUT_{1,j} \left[ |x_1(n-q)| \right] = |x_1(n-q)| \tag{7}
\]

\[
LUT_{2,j} \left[ |x_2(n-q)| \right] = |x_2(n-q)| \tag{8}
\]

The 2D-DPD architecture can be divided into in-band predistorter and out-of-band pre-distorter for each band. Implementation of it based on LUTs can be described as Fig. 2(a).

(a) Conventional architecture based on LUTs

(b) Proposed architecture based on time-division multiplexing with same memory depth

(c) Proposed architecture based on time-division multiplexing with different memory depths
We focus on analyzing from the perspective of only LSB as we can exchange subscripts 1 with 2 to get USB. From the above discussion, we may safely realize that LUT\_{1/m, j} \left[ x_1(n-q) \right] can be viewed as a constant complex gain of \( x_1(n) \) signal envelop and LUT\_{2/j} \left[ x_2(n-q) \right] can be considered as a constant gain of \( x_2(n) \) signal envelop if an arbitrary memory depth \( q \) is fixed. Although transmitted signal is randomly generated in practical system, the range of signal envelop is certain. Such behavior is feasible to pre-store the results which multiply normalized signal envelope of \( x_1(n) \) by extracted pre-distorter coefficients in the LUT\_{1/m, j} \left[ x_1(n-q) \right] table and the normalized signal envelope of \( x_2(n) \) in the LUT\_{2/j} \left[ x_2(n-q) \right] table. The former is retrieved by signal envelope of \( x_1(n) \), the latter is retrieved by signal envelope of \( x_2(n) \). In this paper, the LUT size is 2048, so the normalized minimum resolution is \( \Delta = 1/2 \times 0 \times 2048 \). The form of LUT is shown in Fig. 3.

When pre-distorter memory depth \( q \) is determined, we are aware that the number of LSB and USB needs \( 2K \) of in-band LUTs and \( K \) of out-of-band LUTs by the expression of Eq. (5) and Eq. (7). Considering LSB and USB at the same time, 6\( K \) LUTs are required. Using this approach, the whole pre-distortion system is constructed by creating different memory depth LUTs. The total number of LUTs estimated is 6\( KQ \).

2.3 2D-DPD implementation solution

2.3.1 Time-division multiplexing for out-of-band LUTs with same memory depth

The above-mentioned method has explained that conventional pre-distorter model established by LUTs has saved a lot of hardware resources, as shown in Fig. 2(a). However the conventional pre-distorter which contains too many LUTs whose number will increase severely as the memory depth and nonlinear order increase is not the simplest architecture. In order to reduce hardware resources further, in this paper, a time-division multiplexing concept is introduced.

LUTs are operated in parallel and each operation occupies an entire time slot. Furthermore, contents stored in out-of-band LUTs of LSB and USB do not have coefficients. We can easily detect symmetrical relationships between LSB and USB when memory depth \( q \) is fixed. As shown in Fig. 2(b), we take advantage of time-division multiplexing technology for LSB and USB out-of-band LUTs when memory depth \( q \) is fixed. In this way, the number of out-of-band LUTs will be reduced by half.

We convert out-of-band LUTs from the parallel operation to serial, so the operations of all indexing out-of-band LUTs must be conducted in a serial way. The time sequence of these operations is shown in Fig. 4.
Transforming out-of-band LUTs from parallel process to serial, the time duration for each LUT operation becomes shorter. Here, original data must be up-sampled by a factor 2 and signal processing rate must be conducted twice of original one. After that, the output data are down-sampled by a factor 2. At the end of these operations, output data rate turns to be the original sampling rate. The block diagram of time-division multiplexing out-of-band LUT is shown in Fig. 5. In this way, the number of LUTs that the whole system needs is $5KQ$.

### 2.3.2 Time-division multiplexing for out-of-band LUTs with different memory depths

The conventional architecture of 2D-DPD has been depicted in Fig. 2(a). Out-of-band LUTs are operated in parallel not only between LSB and USB when memory depth $q$ is fixed, but also in one band whose difference between adjacent memory depths is a clock at the same time. In this part, just as shown in Fig. 2(c), time-division multiplexing technique is applied to out-of-band LUTs in LSB or USB.

This method is different from above-mentioned in Sect. 2.3.1 which only employs time-division multiplexing technology in LSB or USB. By this means, the time sequence is similar to the sequence in Fig. 4 and block diagram of time-division multiplexing architecture is similar to the block diagram in Fig. 5. The dual-band input signal envelope must be up-sampled by a factor $Q$. Similarly, the final output signals are down-sampled by a factor $Q$ to get back the original data sampling rate. By such process, the number of LUTs whole system requires can be estimated as $4KQ+2K$.

### 2.3.3 Hybrid time-division multiplexing for out-of-band LUTs

The last method for the implementation of 2D-DPD is a hybrid solution combining method in Sect. 2.3.1 and method in Sect. 2.3.2. Out-of-band LUTs in different memory depths of LSB or USB employ the time-division multiplexing technique, just as the method in Sect. 2.3.2. In addition, LSB and USB use time-division multiplexing technique again, just as the method in Sect. 2.3.1. The block diagram of this implementation is shown in Fig. 2(d).

By this way, the input signal envelope need to be up-sampled by a factor $Q+2$ and the output data must be down-sampled by the same factor $Q+2$ to turn back to the original data sampling rate. The number of LUTs the whole system demands will be $4KQ+4K$. Compared with conventional LUT-based 2D-DPD architecture, the number of LUTs required is significantly reduced.

### 3 Measurement setup and experimental results

#### 3.1 Measurement setup

The performance of 2D-DPD model has already been demonstrated in Ref. [1]. Nonetheless, we are more concerned with the accuracy of this model implemented on hardware. In this paper, we compare hardware-implemented 2D-DPD model using time-division multiplexing method with hardware-implemented 2D-DPD model using conventional method and software-implemented one. The hardware-implemented setup is depicted in Fig. 6(a). It mainly consists of two parts, one is a FPGA development board Virtex-6 produced by Xilinx company, the other is a dual-band transceiver system board imitated with a signal-band one produced by ADI. The dual-band transceiver board possesses two forward paths and two feedback paths which are parallel to process
signal concurrently. Every forward path and feedback path has its own DAC and ADC. Quadrature modulator, filters and some attenuators are distributed in both forward and feedback paths.

Original baseband signal sampling rate is 245.76 million samples per second (Msps). The DAC is a 16-bit accuracy sampling at a rate of 491.52 Msps. After the output digital signal of FPGA development board is interpolated by factor 2 directly by DAC, it will become analog signal. The 12-bit ADC sampling rate at 491.52 Msps is used in feedback paths, as well. The FPGA development board works at 245.76 MHz. Connecting two matched length short sub-miniature-A (SMA) cables from dual-band transceiver board to FPGA development board, which is capable of achieving synchronization of two boards.

In this paper, the digital baseband signals are generated by MATLAB software in the computer and downloaded into FPGA in the form of ROM. In the transmission paths, LSB and USB baseband signals are up-converted to RF of 2.61 GHz and 2.69 GHz. In the feedback paths, the other band RF signal is filtered by a band-pass filter. The filtered signals then is down-converted to an IF of 368.64 MHz. Finally, the IF signals are digitally down-converted to baseband signals. Capturing the forward and feedback signals, concurrently, we go on to align time, extract coefficients and generate LUTs in MATLAB software. Then, the LUTs are loaded into FPGA memories directly. Afterwards, the performance of 2D-DPD on FPGA with hybrid time-division multiplexing technique to significantly reduce hardware resources will be implemented.

The software-implemented setup is shown in Fig. 6(b). The original baseband signal processed by the 2D-DPD model constructed by MATLAB software firstly and then modulated and up-converted by vector signal generator (Agilent MXG N5182A) to RF analog signal which drives PA immediately. The power-amplified signal from PA is sent to vector signal analyzer (Agilent PXA N9030A) after attenuated by attenuators to observe the spectrum changed before and after pre-distortion.

This paper employs high efficiency 20 W GaN class-F PA ($V_{ds}=28$ V, $V_{gs}=5$ V) to testify the performance of 2D-DPD model implemented on FPGA hardware. The PA bandwidth is 100 MHz, center frequency is 2.65 GHz.

### 3.2 Experimental results

In order to obtain acceptable pre-distortion effect, the memory depth $Q$ and nonlinearity order $K$ in 2D-DPD model are enlarged. In this paper, we choose $Q$ as 4 and $K$ as 8 in Ref. [8]. Fig. 7 shows a comparison of output power spectrum for PA without linearization, PA with 2D-DPD implemented in MATLAB software, PA with 2D-DPD implemented on the FPGA hardware using conventional method and PA with 2D-DPD implemented
on the FPGA hardware using hybrid time-division multiplexing method.

![Graph of PA output power spectrum at LSB](image)

![Graph of PA output power spectrum at USB](image)

**Fig. 7** Comparison of PA output power spectrum

Table 1 lists the measured ACPRs. Without DPD, the ACPRs do not satisfy the maximum $-45$ dBc requirement. However, the 2D-DPD linearization method has already compensated for the out-of-band spectrum regrowth and degraded the ACPRs to less than $-59$ dBc. The hardware-implemented output achieves ACPR improvements of $23.9$ dB/24.6 dB for LSB and $23.4$ dB/22.6 dB for USB using hybrid time-division multiplexing method. The NMSE between the hardware-implemented output using hybrid time-division multiplexing method and software-implemented output is approximately $-62.5$ dB for LSB and $-63.2$ dB for USB, and it comparing both implementations is below $-62.5$ dB for LSB and $-63.0$ for USB on FPGA hardware. The experimental results show that implementation on FPGA hardware using hybrid time-division multiplexing method, using conventional method and in MATLAB software can achieve equivalent performance. The hardware-implemented method using hybrid time-division multiplexing technique has the comparable model accuracy and better DPD performance.

### Table 1 Summary of the ACPR performance

<table>
<thead>
<tr>
<th></th>
<th>LSB</th>
<th>USB</th>
</tr>
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<tbody>
<tr>
<td>Without DPD</td>
<td>$-35.3128$</td>
<td>$-34.7468$</td>
</tr>
<tr>
<td>With software DPD</td>
<td>$-59.3031$</td>
<td>$-59.4517$</td>
</tr>
<tr>
<td>(conventional method)</td>
<td>$-59.4517$</td>
<td>$-59.4517$</td>
</tr>
<tr>
<td>With hardware DPD</td>
<td>$-59.2945$</td>
<td>$-59.3898$</td>
</tr>
<tr>
<td>(hybrid method)</td>
<td>$-59.2945$</td>
<td>$-59.3898$</td>
</tr>
</tbody>
</table>

The original digital baseband signals are two single carrier WCDMA signals with 3.84 MHz bandwidth and are quantified 12 bit signed number. The size of the LUT is 2048, and each has 17 bit storage capacity of signed number for in-band LUTs and 16 bit unsigned number for out-of-band LUTs. Resources that Virtex-6 possesses, conventional method utilize and hybrid time-division multiplexing method utilize are shown in Table 2, where 36RAM/FIFO and DSP48E1 represent LUTs and complex multipliers, respectively. It can be clearly seen that the cost of conventional method is highest. Hybrid time-division multiplexing method uses much fewer LUTs whose number is reduced by 29.17% compared with conventional method, but the number of complex multipliers is still the same.

### Table 2 FPGA resources utilization comparison

<table>
<thead>
<tr>
<th></th>
<th>36RAM/FIFO</th>
<th>DSP48E1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-6</td>
<td>416</td>
<td>768</td>
</tr>
<tr>
<td>conventional method</td>
<td>192</td>
<td>446</td>
</tr>
<tr>
<td>hybrid method</td>
<td>136</td>
<td>446</td>
</tr>
</tbody>
</table>

4 Conclusions

The 2D-DPD model implemented on FPGA has been proposed in this paper. Employing LUT mapping approach as a precondition can efficiently reduce hardware resources. Based on this, we try to utilize less hardware resources to obtain the same performance for 2D-DPD pre-distorter. In this paper, we divide two conventional independent dual-band pre-distorter models into three parts, in-band pre-distorter composed of own part as well as out-of-band pre-distorter of parts LSB and USB co-own. Firstly, time-division multiplexing technique is applied to LSB and USB out-of-band LUTs concurrently when memory depth is fixed. Second, this technique is also employed to out-of-band LUTs in LSB or USB when memory depths are different. Finally, the above two methods are combined together, which can utilize out-of-band LUTs to a maximum extent and save 29.17% resources. The
proposed hardware implementation is tested on a FPGA development board (Virtex-6) connected to a dual-band transceiver board. Our validation method compares hardware-implemented 2D-DPD model using time-division multiplexing method with the hardware-implemented 2D-DPD model using conventional method and the ideal software environment implemented one. NMSEs are around $-62$ dB for LSB and $-63$ dB for USB and ACPRs are less than $-59$ dBc, showing a good correlation and feasibility of the FPGA implemented architecture.

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References


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