Design of a fully differential CMOS LNA for 3.1–10.6 GHz UWB communication systems

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Abstract

A fully differential complementary metal oxide semiconductor (CMOS) low noise amplifier (LNA) for 3.1–10.6 GHz ultra-wideband (UWB) communication systems is presented. The LNA adopts capacitive cross-coupling common-gate (CG) topology to achieve wideband input matching and low noise figure (NF). Inductive series-peaking is used for the LNA to obtain broadband flat gain in the whole 3.1–10.6 GHz band. Designed in 0.18 μm CMOS technology, the LNA achieves an NF of 3.1–4.7 dB, an S11 of less than –10 dB, an S21 of 10.3 dB with ±0.4 dB fluctuation, and an input 3rd interception point (IIP3) of –5.1 dBm, while the current consumption is only 4.8 mA from a 1.8 V power supply. The chip area of the LNA is 1×0.94 mm².

Keywords LNA, common gate, capacitive cross coupling, series peaking, UWB

1 Introduction

UWB systems have recently received much attention because of their potential for high-speed wireless communication [1–3]. Two approaches have been proposed to exploit the spectrum of 3.1–10.6 GHz allocated for UWB systems. One is the multi-band orthogonal frequency-division multiplexing (MB-OFDM) UWB [4], and the other is the direct sequence (DS) UWB [5]. Although the standard has not been completed, a front-end wideband LNA is indispensable regardless of the receiver architecture.

The LNA design is one of the biggest challenges for the implementation of a complementary metal oxide semiconductor (CMOS) UWB system because it must show low noise figure (NF), broadband input matching and reasonable flat gain over a large frequency band.

There are several existing solutions for CMOS-based UWB LNA. The distributed amplifier provides good impedance matching performance [6], but it consumes large dc current and chip area. The resistive shunt-feedback amplifier provides good wideband matching and flat gain, but tends to suffer from poor NF and larger power dissipation [7]. The LNA in Ref. [8] adopts a bandpass filter at the input of a cascode LNA for wideband input matching and shows good wideband performance while dissipating small amounts of dc power. However, the filter at the input requires a number of reactive elements, which can lead to a larger chip area and NF degradation in the case of on-chip implementation. The common-gate (CG) LNA adopting noise canceling technique reported in Ref. [9] achieves good input matching and broadband gain in the whole UWB band. However, the components adopted to cancel the noise current of the input transistor will bring noise and deteriorate the NF of the whole LNA. Furthermore, most of the reported UWB LNA adopt single-ended topologies [6–9], which can cause severe 2nd-order nonlinearities. For zero-IF receivers, 2nd-order nonlinearities are very detrimental.

In this article, the gm-boosted CG LNA concept [10] is used in the fully differential capacitive cross-coupling CG LNA. The inductive series-peaking technique is adopted to achieve wideband flat gain. It is shown that the proposed LNA achieves good input matching, low NF, high linearity, and flat broadband power gain, while it consumes relatively low DC power.

2 Capacitive cross-coupling CG LNA

2.1 Analysis of noise and input matching

It is well known that the CG CMOS amplifier has an input impedance of $1/g_{m}$ where $g_{m}$ is the transconductance of the input transistor. The input matching of a CG LNA is easily obtained by setting $1/g_{m}$ to 50 Ω. Hence, the CG LNA shows...
better broadband input matching than the common-source (CS) LNA. However, the noise performance of the CG LNA is limited by the input matching condition. The noise factor $F$ (NF is the decibel equivalent of $F$) of a CG LNA is:

$$F = 1 + \frac{\gamma}{\alpha g_m R_s}$$

(1)

where $\alpha$ and $\gamma$ are bias-dependent noise parameters of MOS transistors, and $R_s$ is the source impedance. When the input matching condition is fulfilled, $F$ is equal to $1 + \gamma / \alpha$. In deep sub-micron CMOS technology, $\gamma / \alpha$ is larger than 2, which indicates that the NF of a CG LNA is larger than 4.7 dB.

From Eq. (1), a direct way to reduce the NF of a CG LNA is to enlarge $g_m$. However, this will deteriorate the input matching performance. The $g_m$-boosted concept is to decouple the noise performance from input matching in a CG LNA.

The input matching of the $g_m$-boosted CG LNA is implemented at a smaller bias current at the condition of $(1+A)g_m R_s = 1$. Smaller bias current also indicates less channel noise current from the input transistor.

The inverting gain can be implemented by an active amplifier to provide larger $A$, but the active amplifier introduces considerable noise itself. This makes passive methods more attractive. In Ref. [10], the inverting gain is implemented by an on-chip transformer, a gain of larger than 1 can be achieved by adjusting the turn ratio between the primary and secondary inductors of the transformer. However, the performances of on-chip transformers are dependent on technology, and the NF may be deteriorated by the parasitic resistance of the inductors.

In this article, the capacitive cross-coupling method [11] is adopted to implement the inverting gain, as shown in Fig. 1(b). The inverting gain $A$ is approximately denoted as:

$$A \approx \frac{C_{g_m}}{C_{g_m} + C_{gs}}$$

(3)

where $C_{gs}$ is the parasitic capacitance between the gate and source nodes of $M_1$ and $M_2$. The inverting gain is about 1 when $C_{g_m} = C_{g_m} >> C_{gs}$. From Eq. (2), this architecture can provide a minimum NF of about 3 dB. An obvious advantage of the capacitive cross-coupling CG LNA is that it is inherently suitable for fully differential operation.

When the parasitic capacitance is taken into consideration, the input impedance of the Fig. 1(b) is:

$$Z_{in} = \frac{1}{(1+A)g_m + s2C_{gs}}$$

(4)

From Eq. (4), the input matching performance will deteriorate at a high frequency because of the parasitic capacitance. To obtain good input matching at the desired UWB frequency band, a pair of inductors must be added at the input node to resonate with the parasitic capacitance, as shown in Fig. 1(c). The best input matching for the circuit in Fig. 1(c) is obtained at the resonance frequency:

$$\omega_s \approx \frac{1}{\sqrt{C_{g_m}L_{S1}}}$$

(5)

The desired input matching performance can be obtained by adjusting $L_{S1}$ and $L_{S2}$ ($L_{S1}=L_{S2}$) to locate $\omega_s$ at the center of the 3.1–10.6 GHz UWB band.

### 2.2 Bandwidth extension

In narrowband applications, the load of LNA is implemented by an LC tank to provide power gain at the resonance frequency of the tank [10,12]. This cannot be used for an UWB LNA, because it cannot provide broadband flat gain in the whole UWB band.

Figure 2 shows 3 topologies of wideband CG amplifiers, where $C_1$ denotes the parasitic capacitance of $M_1$, and $C_2$ denotes the input parasitic capacitance of the next stage (for example, a mixer). The gain of all the amplifiers can be simply expressed as:

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = g_m Z(s)$$

(6)

where $g_m$ represents the transconductance of $M_1$, and $Z(s)$ denotes the transimpedance of the amplifiers. As $g_m$ is approximately constant, the bandwidth is only dependent on $Z(s)$.
The amplifier shown in Fig. 2(a) has a transimpedance of
\[ Z(s) = \frac{R_D}{1 + sR_D C_L} \]  
(7)
where \( C_L = C_1 + C_2 \). The 3 dB bandwidth can be expressed as
\[ \omega_0 = \frac{1}{\sqrt{R_D C_L}} \]
where \( \omega_0 \) is the resonate frequency. The bandwidth can hardly exceed 3 GHz for the amplifier to provide reasonable gain in 0.18 \( \mu m \) CMOS technology.

The amplifier shown in Fig. 2(b) adopts shunt-peaking technique to extend bandwidth [13], which has a \( Z(s) \) of
\[ Z(s) = \frac{R_D}{1 + s(L_D / R_D)} \]  
(8)

The added inductor in Fig. 2(b) introduces a zero in \( Z(s) \) that increases the impedance with frequency, and thus extends the −3 dB bandwidth. According to Ref. [13], when \( R_D C_L / L_D = 1.414 \), the shunt-peaked amplifier can provide a maximum bandwidth extension ratio (BWER) of 1.84 to that of the amplifier shown in Fig. 2(a). However, even though the peaking at maximum BWER is not taken into account, the shunt-peaked amplifier still cannot provide the required bandwidth of 3.1–10.6 GHz.

The principal reason why the shunt-peaked amplifier cannot provide a bandwidth of 3.1–10.6 GHz is that the parasitic capacitance \( C_L \) seen at the drain terminal of M1 is relatively large, which is the sum of \( C_1 \) and \( C_2 \). Therefore, an effective way of extending the bandwidth further is to use an inductor to split the parasitic capacitance, which is the so-called series-peaking technique [13]. The series-peaked amplifier is shown in Fig. 2(c) and its \( Z(s) \) is denoted as:
\[ Z(s) = \frac{R_D}{1 + sR_D (C_1 + C_2) + s^2 L_D C_1} \]  
(9)

Generally, it is difficult to find the optimum device parameters in Eq. (9) to provide a maximum BWER through computation. Instead, the graphical method can be used. Since \( R_D \) determines the low-frequency gain, and \( C_1 \) and \( C_2 \) are parasitic capacitors, it is reasonable to change the value of \( L_D \) to optimize the bandwidth. Figure 3 shows the normalized frequency response of the series-peaked impedance with different values of \( L_D \).

As seen from Fig. 3, although the required bandwidth can be obtained when \( L_D \) is about 3 nH, the peaking introduced by the resonance makes the impedance fluctuate extensively, which is unacceptable for UWB application.

However, if the series-peaked load is used for the capacitive cross-coupling CG LNA shown in Fig. 1(c), the fluctuation will be compensated by the effective input voltage. As stated above, the input impedance of the LNA in Fig. 1(c) shows a parallel resonant characteristic, as denoted by Eq. (5). Therefore, the effective input volatge is at the maximum under the resonant frequency \( \omega_0 \), while rolling off remarkably at either sides of \( \omega_0 \). We use this characteristic to compensate the fluctuation in the series-peaked impedance, and the required broadband flat gain can be obtained. Figure 4 shows the normalized effective input volatge, output impedance, and overall gain of the capacitive cross-coupling CG LNA adopting series-peaked loads. Additionally, the peaking of the gain at high frequency shown in Fig. 4 will be further attenuated in practical circuits because of the parasitic resistance of on-chip inductors.

3 Circuit design

The full schematic of the proposed fully differential LNA is shown in Fig. 5. The circuit consists of a capacitive-coupling CG LNA core with series-peaked loads. A differential buffer implemented with a source follower is added for measurement. The input impedance matching is achieved by adjusting the size and bias current of M1 and M2 to ensure \( L_\text{in} = 50 \Omega \). The inductors \( L_{D1} \) and \( L_{D2} \) are added to resonate with the gate-source capacitors at the UWB frequency band. The cross-coupling capacitors \( C_{C1} \) and \( C_{C2} \) are implemented with 10-pF metal-insulator-metal (MIM) capacitor. The cascode transistors M3 and M4 are used to improve the reverse isolation of the LNA. The series-peaked load network consists of \( R_0 \), \( R_{D1} \) and \( R_{D2} \), and the parasitic capacitance of M3 (M4) and M5 (M6). The coupling capacitors, \( C_3 \) and \( C_4 \), have relatively large values, and thus the value of \( C_3 \) in Fig. 2(c)
is mainly determined by M5 and M6. To provide output matching at the desired UWB frequency, on-chip inductors $L_{O1}$ and $L_{O2}$ are adopted in the output buffer to resonate with the gate-source parasitic capacitance of M5 and M6. The design parameters of all the instances in Fig. 5 are shown in Table 1.

The chip layout of the LNA is designed with TSMC 0.18 μm CMOS technology and shown in Fig. 6. The chip area is $1 \times 0.94 \text{ mm}^2$.

4 Post-layout simulation results and analysis

The simulation is implemented with Spectre after layout design and parasitic extraction. Two ideal baluns are used to obtain the performance of the fully differential LNA. The simulated NF, $S_{11}$, $S_{12}$, and $S_{22}$ of the LNA are shown in Figs. 7(a) and (b). With the capacitive cross-coupling method, the NF of the LNA is 3.1–4.7 dB in the whole 3.1–10.6 GHz UWB band. The LNA achieves an $S_{11}$ of 9.9–10.7 dB, an $S_{12}$ of below –10 dB, an $S_{22}$ of less than –50 dB, and an $S_{22}$ of less than –10 dB. The simulation results show that the desired low NF, broadband flat gain, input/output impedance matching, and good reverse isolation are obtained from the LNA.

Two-tone RF signals are used to simulate the linearity performances of the LNA. Figure 7(c) shows the simulated input IP3 (IIP3) when the RF frequencies are at 6.55 GHz and 6.45 GHz. The IIP3 is –5.1 dBm, which meets the system requirement [3].
The LNA core consumes 2.6 mA while the buffer consumes 2.2 mA from 1.8 V power supply. The total power consumption is 8.6 mW. Table 2 summarizes the performance of the proposed LNA, with comparison to some published CMOS LNAs. Considering performance degradation after fabrication, the NF and power consumption of the proposed LNA are still the least, while the other performances are medium compared with other LNAs in Table 2.

Table 2  Performance summary and comparison

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5 Conclusions

This article presents a fully differential CG LNA that adopts capacitive cross-coupling architecture for 3.1–10.6 GHz UWB receivers. The inductive series-peaking technique is adopted in the LNA to achieve wideband flat gain. Post-simulation results show that the proposed LNA achieves good input matching, low NF, high linearity, and stable gain, while it consumes relatively low dc power. Designed in 0.18 µm CMOS technology, the LNA consumes 4.8 mA from a 1.8 V power supply, and the chip area is $1 \times 0.94$ mm².

Acknowledgements

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References